A NOVEL 4-18 GHz MONOLITHIC MATRIX DISTRIBUTED AMPLIFIER

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ABSTRACT

This paper describes the design, fabrication, and performance of a 4 to 18 GHz matrix distributed amplifier. This amplifier incorporates a novel biasing scheme which enables the stages to be connected in cascade at RF frequencies and in cascode for dc biasing, thus conserving current. This is the first MMIC amplifier of its kind. The amplifier has shown greater than 13 dB gain across the frequency band.

INTRODUCTION

As distributed amplifiers [1-3] are gaining popularity in microwave broadband integrated circuits applications, a variant of the distributed amplifier, the matrix amplifier [4-6], has recently been described. In this circuit, chains of distibuted amplifiers, having inherently large gain-bandwidth products, are stacked such that the output artificial transmission line of one chain is shared with the input artificial transmision line of the next chain, giving rise to an idle line which is RF terminated at both ends. This construction is very compact and offers circuits with higher gain per unit area than can be achieved with conventional cascaded multistage distributed amplifiers. Figure 1 shows a comparison of the block diagrams of a matrix distributed amplifier and a conventional cascaded multistage amplifier, each amplifier having two 5-FET chains.

Many systems applications can accommodate only a fixed supply voltage, and in these cases, dc current consumption is an important design issue. The matrix distributed amplifier described in this paper incorporates a biasing scheme which enables the amplifier to run at these higher voltages while drawing only half of the current of conventional multistage amplifiers having comparable gain levels.

AMPLIFIER DESIGN

Two matrix distributed amplifiers were designed and fabricated. The two versions differ only in their biasing schemes so they provide similar performance at microwave frequencies. The total gate periphery of each version is 1.6 mm, and each amplifier consists of ten 160 μm FETs in two chains. Figure 2 shows the schematic of the first version. The idle ports of both input and output artificial transmission lines are terminated with load resistors to provide an adequate return loss. The center line serves as the output line of the first chain and as the input line of the second chain. The idle ports of the center line are also terminated with load resistors.

To demonstrate the biasing scheme of the amplifier, consider the pair of FETs shown in Figure 3. The two FETs are cascode connected at dc through an inductor L_B. At RF, this same inductor provides isolation between the FETs, and C_B effectively grounds the source of FET2. Both circuit elements are needed to allow the two FETs to be operated as cascaded amplifiers.

Since the output FET of the pair, FET2, can only run at I_{dss}, FET1 must also be biased close to I_{dss}. Amplifier performance is, therefore, very sensitive to the gate voltage applied to the input FET, FET1, and to the uniformity of the dc characteristics of the two FETs. In Figure 4, points A and B show how the resulting transconductance of the FET pair can be compressed near I_{dss} when the I_{dss} of FET2 is much lower than that of FET1.

To overcome this problem, the second amplifier version which employs a voltage divider at the input of the FET pair was also designed and fabricated. Figure 5 shows the same FET pair, but now with a voltage divider to derive the gate bias, ensuring that both FETs are biased at the same point. The schematic of the version 2 amplifier is shown in Figure 6.

Figure 7 shows the predicted performance of the version 1 amplifier. Predicted gain is 15 dB ± 1 dB and input and output return losses are better than -7 dB. The predicted gain is higher than that of two conventional cascaded amplifiers of similar gate periphery because total loss associated with the propagation of the signal along the artificial transmission lines has been reduced. This is a consequence of the sharing of two of these lines.

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IC FABRICATION

The matrix distributed amplifiers were fabricated on a 4 mil thick semi-insulating GaAs substrate. Figure 8 is a photograph of version 1 and Figure 9 is a photograph of version 2. The sizes of the chips are 74 mil x 83 mil. All dc bias circuitry is incorporated on the chips. The gates of the FETs are 0.5 μm long and the active layer was formed by blanket ion implantation such that a doping level of 2×10^{17} cm^{-3} was obtained. Oxygen implantation and shallow etching provide the mesa isolation. Capacitors are MIM structures with 2000 A of CVD Si_3N_4 as the dielectric. Resistors are made of 4000 A of sputtered tantalum. Spiral inductors with 5 μm line to line spacings are used throughout the amplifier design to form a compact die size.

MEASURED PERFORMANCE

The small signal performance of the version 1 amplifier, when biased at 7 V on the drain of the FET pair, is shown in Figure 10. Measured gain is 14 dB ± 1.5 dB from 4 GHz to 18 GHz. Measured input and output return losses are better than -7 dB over the band. Figure 11 shows the measured power performance of the same amplifier biased at 7 V and at 10 V on the drain of the FET pair. At 7V, measured power is better than 15 dBm from 4 GHz up to 16.5 GHz at the 2 dB compression point. Power drops down to 13 dBm at 18 GHz. At 10V, power is better than 18 dBm over the complete frequency band. Figure 12 shows the performance of the version 2 amplifier, also biased at 7 V on the drain of the FET pair, and with -1 V on the gate. Measured gain is 11 dB ± 1 dB over the band. Measured input and output return losses are better than -7 dB.

CONCLUSION

A 4 GHz to 18 GHz monolithic matrix distributed amplifier with a novel biasing scheme has been demonstrated. A gain of 14 dB ± 1.5 dB has been measured over this frequency band in a chip area of only 1.9 mm X 2.1 mm. The success of this work has paved way to the development of a new family of high gain, compact, broadband amplifiers.

ACKNOWLEDGEMENTS

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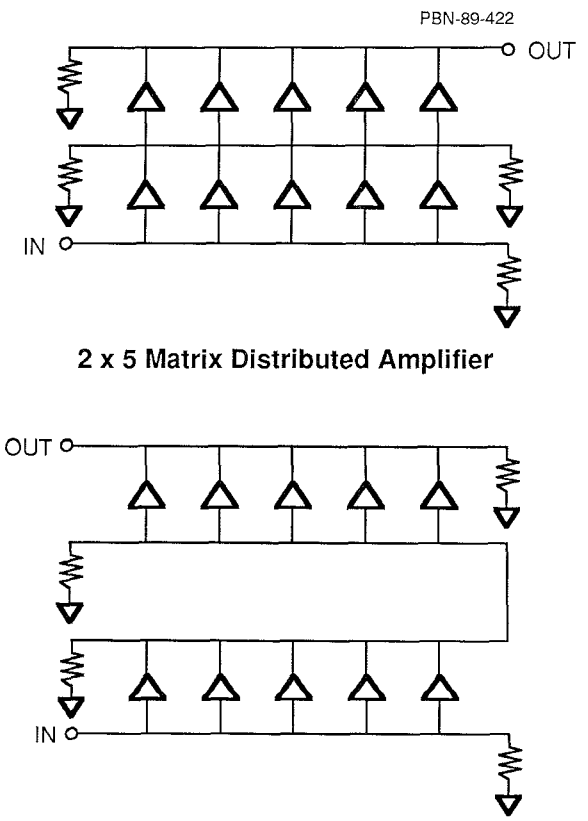

Figure 1. Comparison of Block Diagrams of Matrix Distributed Amplifier and Conventional Cascaded Distributed Amplifier.

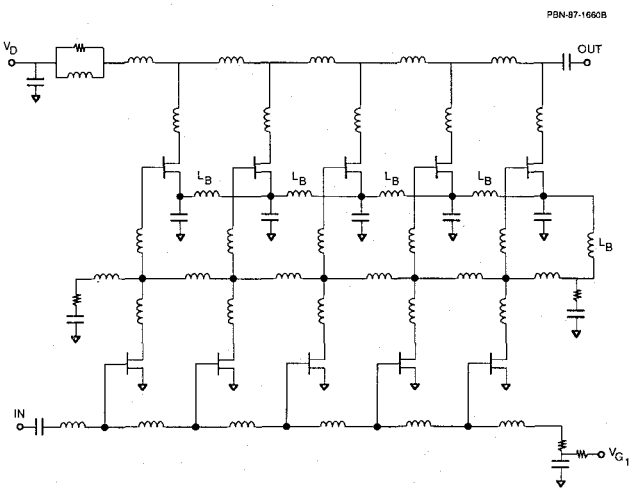

Figure 2. Schematic of Version 1 Matrix Distributed Amplifier.

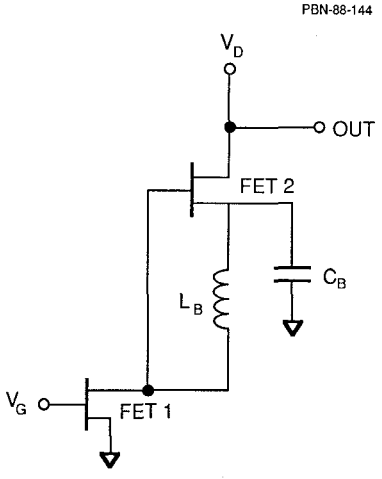

Figure 3. Biasing Scheme of Version 1 Matrix Distributed Amplifier.

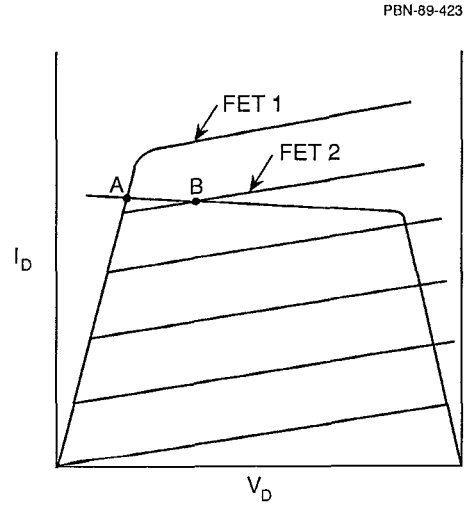

Figure 4. Compression of Transconductance Near I_{dss}.

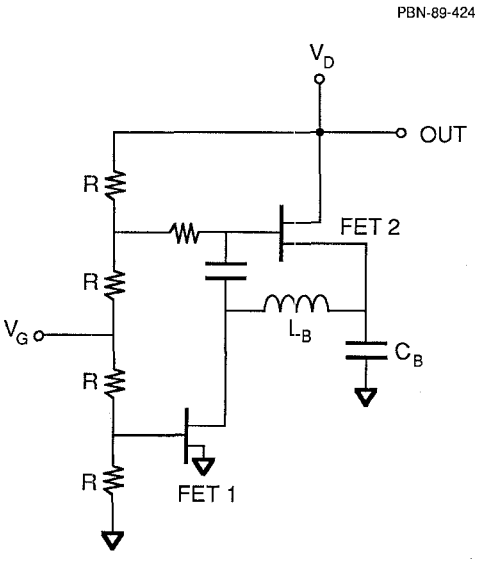

Figure 5. Biasing Scheme of Version 2 Matrix Distributed Amplifier.

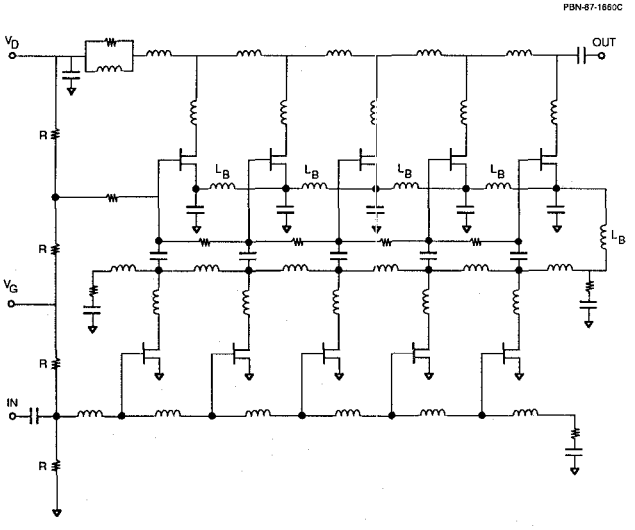

Figure 6. Schematic of Version 2 Matrix Distributed Amplifier.

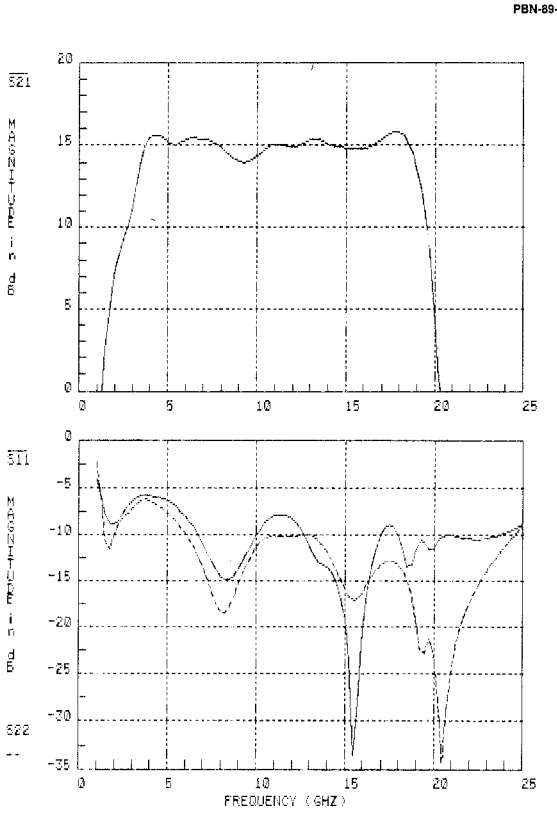

Figure 7. Predicted Performance of Version 1 Matrix Distributed Amplifier.

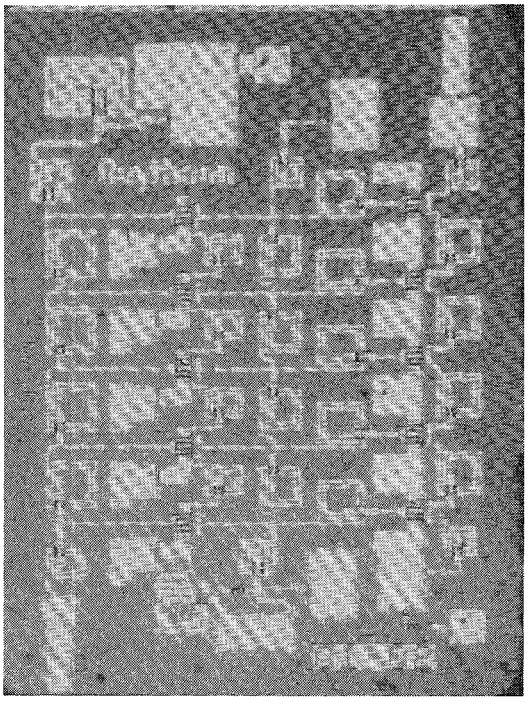

Figure 8. Photograph of Version 1 Matrix Distributed Amplifier.

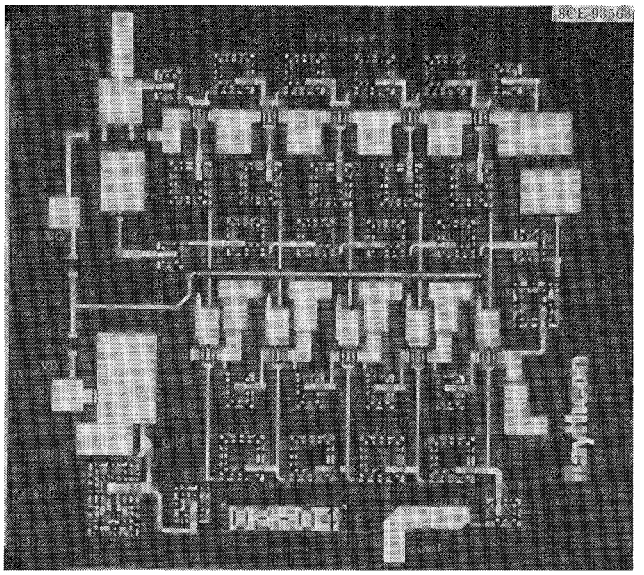

Figure 9. Photograph of Version 2 Matrix Distributed Amplifier.

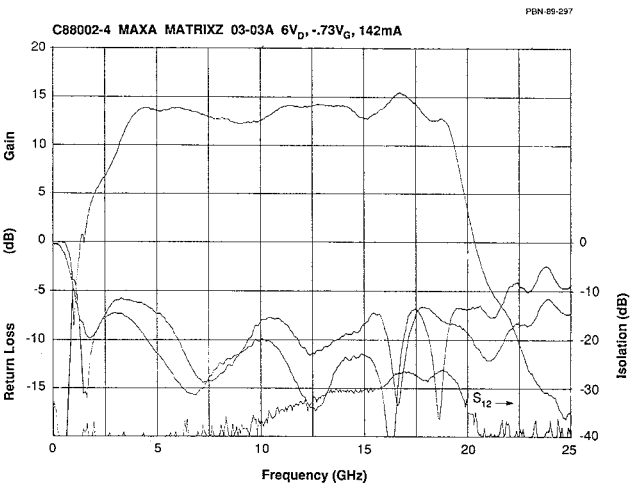

Figure 10. Measured Performance of Version 1 Matrix Distributed Amplifier.

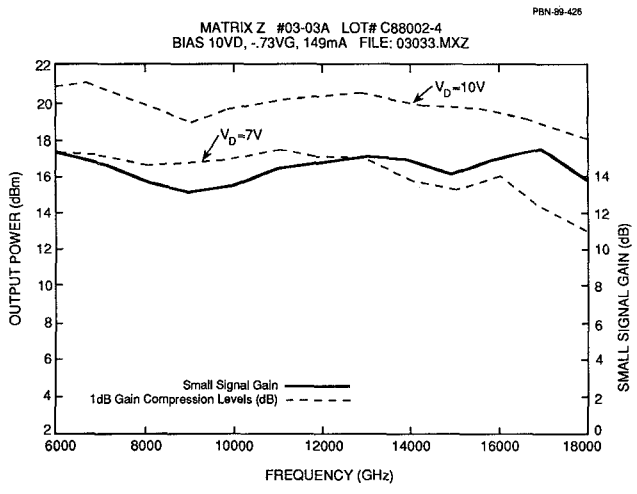

Figure 11. Measured Power of Matrix Distributed Amplifier.

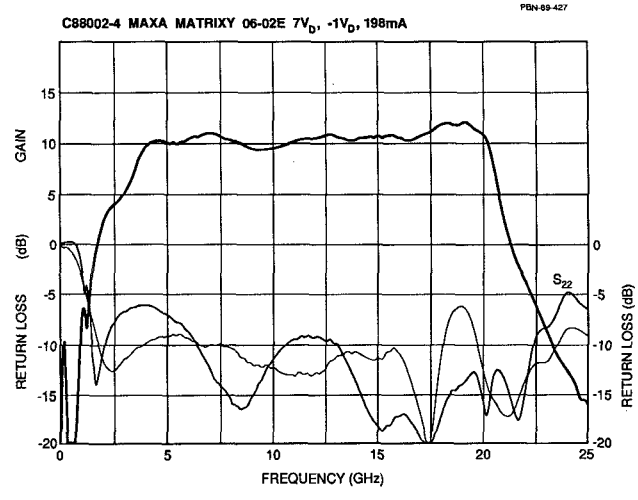

Figure 12. Measured Performance of Version 2 Matrix Distributed Amplifier.